REMARKS

[1] The title is amended. Withdrawal of the objection is requested.

[2] The specification was objected to. However, the Examiner required amendment of the drawing, and the Applicant understands that the Examiner was not requiring any amendment to the specification.

The objection is respectfully traversed on the basis that Fig. 3 already illustrates what is asserted to be lacking. In Fig. 3, the first conductivity type transistors are the transistors 10 and 11, which also appear in Fig. 1(a), is given as first conductivity type at page 9, line 25; that transistors 10 and 11 are both of this type is shown by the orientation of their arrows, which both point in to indicate the P-well 22 (see Fig. 1(b)). Conversely, transistors 17 and 18, with their arrows pointing out, are automatically of the second conductivity type and therefore include N-wells corresponding to the P-wells illustrated in Figs. 1(a) (by arrows) and Fig. 1(b) (by numeral 22). Transistor 17 is the analogue of protection transistor 10, and therefore it is the protection resistor of the second conductivity type.

Parsing and considering the text which the Examiner asserts is not supported in the drawing, the Applicant now asks the Examiner to consider:

(1) As to the *second-conductivity-type MOS protection transistor having a drain connected to the drain of said second-conductivity-type MOS output transistor,* the Examiner is invited to consider the attached photocopy of Fig. 3 where this connection is indicated by the lower yellow highlighted path.

(2) As to *a source connected to a source of said second-conductivity-type MOS output transistor,* the source of transistor 17 is connected to the source of transistor 18 through the upper highlighted path in Fig. 3.

(3) As to *a gate connected to a first-conductivity-type layer under a gate of said second-conductivity-type MOS output transistor,* the Examiner is invited to consider the middle highlighted path on the attached photocopy of Fig. 3 and the specification at page 11, line 10,

which reads: "In this case, as shown in FIG. 3, on a PMOS output transistor 18 side, the gate [heavy vertical line] of a PMOS protection transistor 17 and a N-well of the PMOS output transistor [arrow leading out from PMOS transistor 18] are connected."

Withdrawal of the objection is requested.

[3] The drawing was objected to. Figs. 6-8 are labeled as "Related Art" in accordance with the heading at page 1, line 9. Approval and withdrawal of the objection are requested.

The Applicant submits amendments to Figs. 1 and 2 which add reference numerals for completeness. Support is found in the specification at page 11, line 8. No new matter is entered. Approval is requested.

[4-5] Claim 1 was rejected under §102(a) as being anticipated by the Applicant's admitted prior art (APA). This rejection is moot because claim 4 is now combined into claim 1. The rejection of claim 4 is addressed below.

[6-7] Claims 1, 4, and 5 were rejected under §102(e) as being anticipated by Sugerman '840. This rejection is respectfully traversed. The Applicant's amended claim 1, as exemplified in the drawing, recites

> *A semiconductor apparatus* [Figs. 1-3] *which protects a first-conductivity-type MOS output transistor* [11] *against a surge entering through an output electrode* [12] *connected to a drain* [upper terminal in Fig. 1(a); 25 in Fig. 1(b)] *of said first-conductivity-type MOS output transistor, said apparatus comprising:*
>
> *a first-conductivity-type MOS protection transistor* [10] *having a drain* [upper terminal in Fig. 1(a); 15 in Fig. 1(a)] *connected to the drain* [25] *of said first-conductivity-type MOS output transistor, a source* [lower terminal in Fig. 1(a); 16] *connected to a source* [26] *of said first-conductivity-type MOS output transistor, and a gate* [heavy vertical line in Fig. 1(a); 14 in Fig. 1(a)] *connected to a second-conductivity-type layer* [22 in Fig. 1(b)] *under a gate* [21 in Fig. 1(b)] *of said first-conductivity-type MOS output transistor;*

wherein the gate [14] *of said first-conductivity-type MOS protection transistor is connected by an electrode wiring* [28, amended Fig. 1(b)] *to said second-conductivity-type layer under the gate* [21] *of said first-conductivity-type MOS output transistor.*

The claimed metal path 28 improves the performance (please refer to page 15, lines 8-20). The features of the last paragraph, which were originally in claim 4, are not found in the prior art.

The Examiner asserts that Sugerman anticipates the features of the last paragraph by gate 170 of the protection resistor M11 being connected by electrode wiring to the layer 140 under the gate 160 of the output transistor M10, as shown in Fig. 5.

The Examiner is invited to note that the Applicant's Fig. 1(a) differs from Sugerman's Fig. 4 in showing the two transistors being similarly oriented, while in Sugerman's Fig. 4 the transistors are oriented as in mirror images. This means that in Sugerman's drawing there is no direct path from the gate of the protection resistor M11 to the gate of the output transistor M10, while the Applicant's Fig. 1(a) shows the gate 14 of protection transistor 10 being directly coupled to the P-well 27 of the output transistor 11. The Applicant's specification notes this: "A gate electrode 14 of the NMOS dummy transistor 10 is connected to the P-well 22 via the P+ contact layer 27 of the NMOS output transistor 11" (page 10, line 13).

The connection is made via the electrode wiring 28, which is now labeled in Figs. 1(b) and 2.

Sugerman's Fig. 4, which shows the same structure as applied Fig. 5 (col. 5, lines 31-33), does not disclose the feature of claim 1 in italics above. Instead, the gate of Sugerman's protection transistor M11 is connected directly to the gate of output transistor M10; Sugerman so states at col. 6, lines 8-9. There is also a branch to one side of resistor R10. In applied Fig. 5, this side is the right-hand side of resistor R10 (noting the position of pad 30 in Figs. 4 and 5). Fig. 5 shows this side of the resistor being connected to gates 170 and 160 (also shown in Fig. 4, as mentioned above) and contacts 220, both of which are adjacent to the PWell 140.

However, these contacts 220 are not in direct contact with the PWell 140 and therefore they are not "connected" to the PWell 140. What they *are* connected to is the source 200 (col. 6, line 41) and a "bulk region" 210 (col. 6, line 46) which is identical in appearance to the source 200 and drain 190. Thus, the gate is not "*connected by an electrode wiring to said second-conductivity-type layer* [140] *under the gate* [160] *of said first-conductivity-type MOS output transistor* [M10]" as claimed, and there is no anticipation of this feature.

The word "connected" implies that there is nothing intermediate. New claim 31 makes this feature more explicit by reciting that the connection of claim 1 is "direct."

[8-9] Claims 2, 3, and 6-15 were rejected under §103(a) as being unpatentable over Sugerman in view of Staab '790. This rejection is respectfully traversed on the basis of the arguments above for claim 1, from which those claims depend.

[10] The allowance of claims 16-30 is noted with appreciation. Withdrawal of the rejections, and allowance of the remaining claims, is requested.

Respectfully submitted,

November 1, 2005
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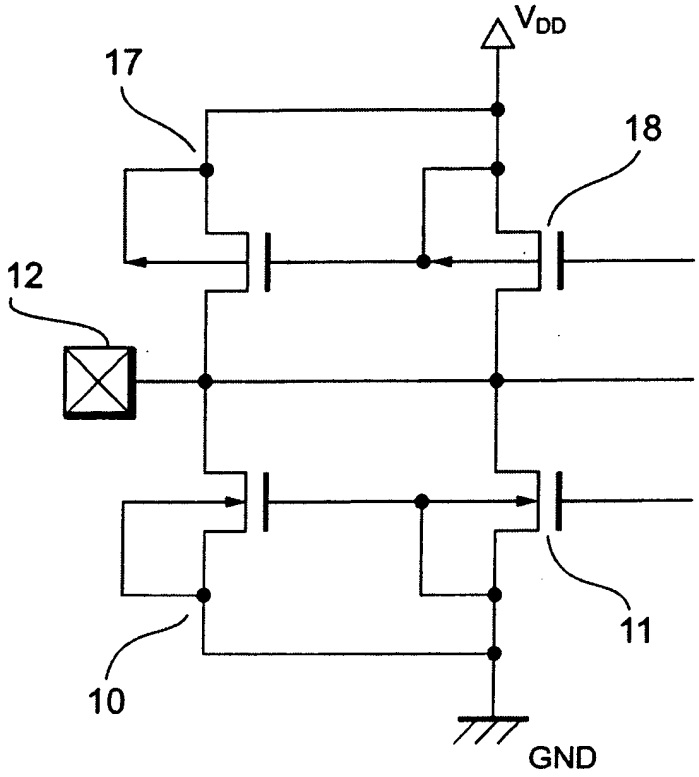
Fig.3



NOT A DRAWING CHANGE

DO NOT ENTER